Logical Instructions AND, NOT, OR, XOR

Using Logical Instructions

These instructions (Table 5.A) perform logical operations.

Table 5.A
Available Logical Instructions

If You Want to:	Use this Instruction:	Found on Page:
Perform an AND operation	AND	5-2
Perform a NOT operation	NOT	5-3
Perform an OR operation	OR	5-4
Perform an XOR operation	XOR	5-5

The parameters you enter are program constants or direct logical addresses.

For more information on the operands (and valid data types/values of each operand) used by the instructions discussed in this chapter, see Appendix C.

Using Arithmetic Status Flags

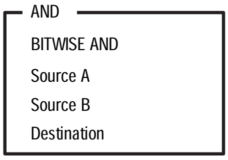
The arithmetic status bits are in word 0 bits 0-3 in the processor status file (S). Table 5.B lists the status flags:

Table 5.B
Arithmetic Status Flags

This Bit:	Description:
S:0/0	Carry (C)
S:0/1	Overflow (V)
S:0/2	Zero (Z)
S:0/3	Sign (S)

AND Operation (AND)

Description:



Use the AND instruction to perform an AND operation using the bits in the two source addresses.

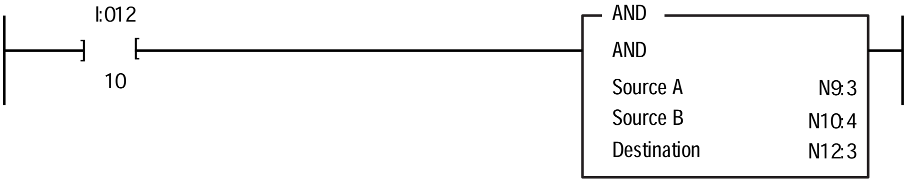
Table 5.C
Truth Table for an AND Operation

Source A	Source B	Result
0	0	0
1	0	0
0	1	0
1	1	1

Table 5.D
Updating Arithmetic Status Flags for an AND Instruction

With this Bit:	The Processor:
Carry (C)	always resets
Overflow (V)	always resets
Zero (Z)	sets if result is zero; otherwise resets
Sign (S)	sets if most-significant bit is set; otherwise resets

Example:

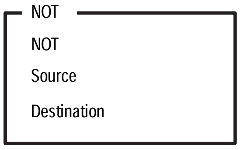


If input word 12, bit 10 is set, the processor performs an AND operation on N9:3 and N10:4 and stores the result in N12:3.

Source A N9:3	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
Source B N10:4	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1
Destination N12:3	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0

NOT Operation (NOT)

Description:



Use the NOT instruction to perform a NOT operation using the bits in the source address. This operation is also know as a bit inversion.

Important: The NOT instruction is not available on PLC-5/15 series A processors.

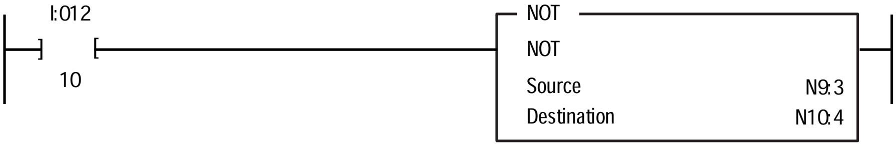
Table 5.E
Truth Table for a NOT Operation

Source	Result
0	1
1	0

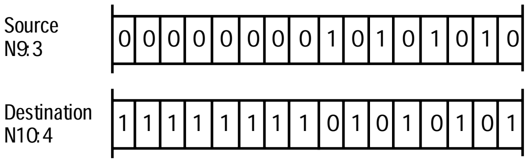
Table 5.F
Updating Arithmetic Status Flags for a NOT Instruction

With this Bit:	The Processor:
Carry (C)	always resets
Overflow (V)	always resets
Zero (Z)	sets if result is zero; otherwise resets
Sign (S)	sets if most-significant bit is set; otherwise resets

Example:



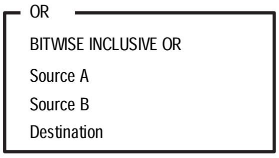
If input word 12, bit 10 is set, the processor performs a NOT operation on N9:3 and stores the result in N10:4



Source N9:3	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
Destination N10:4	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1

OR Operation (OR)

Description:



Use the OR instruction to perform an OR operation using the bits in the two sources (constants or addresses).

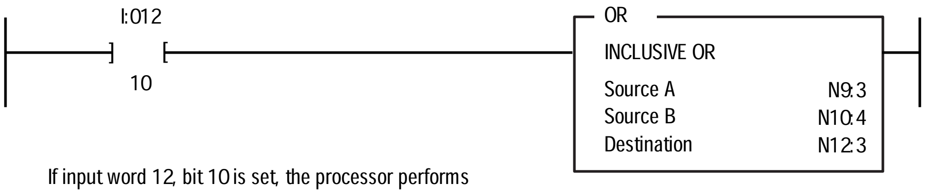
Table 5.G
Truth Table for an OR Operation

Source A	Source B	Result
0	0	0
1	0	1
0	1	1
1	1	1

Table 5.H
Updating Arithmetic Status Flags for an OR Instruction

With this Bit:	The Processor:
Carry (C)	always resets
Overflow (V)	always resets
Zero (Z)	sets if result is zero; otherwise resets
Sign (S)	sets if most-significant bit is set; otherwise resets

Example:

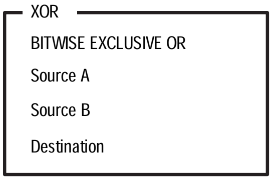


If input word 12, bit 10 is set, the processor performs an OR operation on N9:3 and N10:4 and stores the result in N12:3.

Source A N9:3	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
Source B N10:4	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1
Destination N12:3	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1

Exclusive OR Operation (XOR)

Description:



Use the XOR instruction to perform an exclusive OR operation using the bits in the two sources (constants or addresses).

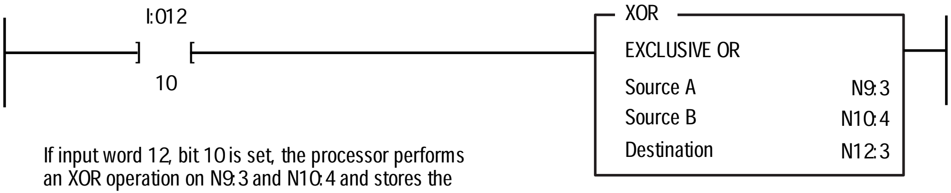
Table 5.I
Truth Table for an XOR Operation

Source A	Source B	Result
0	0	0
1	0	1
0	1	1
1	1	0

Table 5.J
Updating Arithmetic Status Bits for an XOR Instruction

With this Bit:	The Processor:
Carry (C)	always resets
Overflow (V)	always resets
Zero (Z)	sets if result is zero; otherwise resets
Sign (S)	sets if most-significant bit is set; otherwise resets

Example:



If input word 12, bit 10 is set, the processor performs an XOR operation on N9:3 and N10:4 and stores the result in N12:3.

Source A N9:3	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
Source B N10:4	0	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1
Destination N12:3	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1

Notes: